REMARKS

Applicants appreciate the Examiner's thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Claims 2-21 are pending in the application. Claim 1 has been canceled. Claim 4 has been rewritten in independent form including all limitations of base claim 1. Claims 2, 5-7 have been amended to depend from claim 4. Claim 5 has been further amended to better define the claimed invention. New claims 8-21 have been added to provide Applicants with the scope of protection to which they are believed entitled. The specification has been revised to correct a minor typographical error. FIGs. 2-3 have been amended to overcome the Examiner's drawing objection. No new matter has been introduced through the foregoing amendments.

The objection to the drawings is believed overcome in view of the above amendments.

The *35 U.S.C. 102(b)* rejection of claims 1-4 and 6 as being anticipated by *Marrs* (U.S. Patent No. 5,583,378) is noted. Applicants respectfully traverse the rejection of claim 4 as the applied reference clearly fails to teach or disclose each and every element of the rejected claim, i.e., either (i) a plurality of chip contact pads formed on the surface of the insulating layer (claim 1) or (ii) a plurality of conductive vias formed through the insulating layer. The Examiner alleged that the latter is found in FIG. 2A, element 220, and described in column 8 of *Marrs*. It appears that the Examiner is reading layers 214 and plated vias 220 of *Marrs* on the claimed insulating layer and conductive vias, respectively. Assuming that the Examiner's reading of the reference was correct, the so read reference would then fail to teach the former limitation because the *Marrs* chip contact pads 306 are not formed on the surface of the insulating layers 214.

The advantage of the structure claimed in claim 4 is described in the specification, e.g., page 4 line 26 through page 5 line 2. In particular, it has been disclosed that a metal coating 310 is formed

on the lower surface of the substrate 210 **and a plurality of conductive vias 320 are formed through the reinforcement-containing insulating layer 211**. Thus, the heat generated from the semiconductor chip 220 can be conducted to the metal coating 310 through **the conductive vias 320**, and then dissipated to the outside environment through the metal coating 310 thereby enhancing the thermal performance of the package. **Thus, the heat generated from the semiconductor chip 220 is directly conducted to the metal coating 310 through the conductive via 320.**

Marrs fails to achieve the disclosed advantage. In particular, FIG. 3 of Marrs et al., is disclosed that an insulating layer 306 is applied with adhesive to thermal conductor first surface 305. Conductive trace layer 338 is then applied over insulating layer 306. The two layers 306 and 338 present a minimal thermal barrier between integrated circuit chip 302 and thermal conductor 304. If too many layers 306 and 338 are applied, they can increase the thermal resistance between integrated circuit chip 302 and thermal conductor 304 and hinder heat dissipation from integrated circuit chip 302. **Thus, the heat generated from the integrated circuit chip 302 cannot be directly conducted to the thermal conductor 304.**

Accordingly, Applicants respectfully submit that *Marrs* does not anticipate claim 4 which has been rewritten in independent form including all limitations of base claim 1, now cancelled. Claims 2-3 and 5-7 have been amended to depend from claim 4 and are thus patentable over the applied references, notwithstanding the *35 U.S.C. 103(a)* rejections manifested in paragraphs 5-6 of the Office Action.

New claims 8-10 and 21 depend from claim 4, and are considered patentable for at least the reason advanced with respect to claim 4. Claims 9-10 are also patentable on their own merits as these claims recite other features of the invention neither disclosed, taught nor suggested by the applied art. In particular, as to claims 9-10, *Marrs* clearly fails to disclose, teach or suggest that conductive vias that extend **from the metal coating**, through the insulating layer, to said conductive traces. Elements

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,
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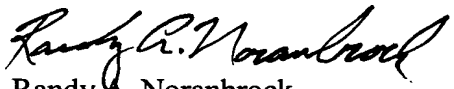

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